

WHAT IS CLAIMED IS:

- 1 1. A method of processing a wafer, comprising:
2 providing a wafer having initial thickness variations between two
3 surfaces of said wafer;
4 processing said wafer through a first module, said first module
5 comprising apparatus for performing a grinding process, a clean process and a metrology
6 process, and said processing therethrough includes said grinding process, said clean process
7 and said metrology process;
8 defining an edge profile on said wafer; and
9 processing said wafer through a second module, said second module
10 comprising apparatus for performing a double side polish (DSP) process, a clean process and
11 a metrology process, and said processing therethrough includes said DSP process, said clean
12 process and said metrology process.
- 1 2. The method of claim 1 wherein said first module processing further
2 comprises an etch process, said etch process reducing said wafer thickness by less than about
3 ten (10) microns.
- 1 3. The method of claim 1 wherein said first module processing precedes
2 said defining said edge profile.
- 1 4. The method of claim 1 wherein said first and second modules each
2 comprise a cluster tool defining a clean room environment.
- 1 5. The method of claim 1 wherein said first module metrology process is
2 simultaneous with said grinding process.
- 1 6. The method of claim 5 wherein said first module metrology process
2 produces a metrology profile for said wafer, said processing through said first module further
3 comprising modifying said grinding process in response to said metrology profile.
- 1 7. The method of claim 1 wherein said first module metrology process is
2 after said grinding process.
- 1 8. The method of claim 1 further comprising polishing said edge of said
2 wafer after said defining said edge profile.

1 9. The method of claim 1 further comprising processing said wafer
2 through a third module, said third module comprising apparatus for performing a finish polish
3 process, a clean process and a metrology process, and wherein said processing through said
4 third module comprises said finish polishing process, said clean process and said metrology
5 process.

1 10. The method of claim 9 further comprising, after completion of said
2 processing through said third module, providing said wafer directly to a process chamber for
3 fabrication of a semiconductor device.

1 11. The method of claim 9 further comprising, in order after completion of
2 said processing through said third module, cleaning said wafer, inspecting said wafer,
3 packaging said wafer, and delivering said wafer to a wafer process facility for subsequent
4 fabrication of a semiconductor device.

1 12. The method of claim 1 wherein said wafer has a total thickness
2 variation (TTV) between said two surfaces of less than about 0.3 microns after said
3 processing through said second module.

1 13. The method of claim 1 wherein said wafer has a SFQR of less than
2 0.12 microns after said processing through said second module.

1 14. The method of claim 1 further comprising processing said wafer
2 through at least a portion of said first module prior to processing a second wafer through said
3 first module.

1 15. The method of claim 1 further comprising laser marking said wafer
2 prior to said defining said edge profile.

1 16. The method of claim 1 further comprising performing a donor anneal
2 process prior to said defining said edge profile.

1 17. The method of claim 1, further comprising processing said wafer
2 through a third module, said third module comprising apparatus for performing said defining
3 said edge profile, and an edge polishing process, said processing through said third module
4 comprising said defining said edge profile and said polishing said wafer edge.

1 18. A method of processing a wafer prior to device formation thereon, said
2 method comprising, in order:
3 providing a wafer having first and second surfaces and a peripheral
4 edge;
5 grinding said first and second wafer surfaces;
6 defining an edge profile of said wafer, and polishing said peripheral
7 edge; and
8 polishing said first and second wafer surfaces.

1 19. A wafer processing system, comprising:
2 a grinder for grinding first and second wafer surfaces;
3 an etcher for etching said wafer;
4 a cleaner for cleaning said wafer; and
5 a metrology tester for testing a metrology of said wafer;
6 wherein said grinder, etcher, cleaner and metrology tester are
7 contained within a first clean room environment.

1 20. The wafer processing system as in claim 19 further comprising a
2 transfer mechanism adapted to transfer said wafer from said grinder to said etcher within said
3 first clean room environment.

1 21. The wafer processing system as in claim 20 wherein said transfer
2 mechanism comprises a robot.

1 22. The wafer processing system as in claim 19 further comprising a
2 second clean room environment, said second clean room environment comprising:
3 an edge grinder for defining an edge profile of said wafer; and
4 an edge polisher for polishing said wafer edge.

1 23. The wafer processing system as in claim 19 further comprising a third
2 clean room environment, said third clean room environment comprising:
3 a polisher for polishing said wafer;
4 a cleaner for cleaning said wafer; and
5 a metrology tester for testing said wafer metrology.

1 24. The wafer processing system as in claim 19 further comprising a fourth
2 clean room environment, said fourth clean room environment comprising:
3 a finish polisher for polishing said wafer;
4 a cleaner for cleaning said wafer; and
5 a metrology tester for testing said wafer metrology.

1 25. A wafer processing system, comprising:
2 means for grinding said wafer;
3 means for cleaning said wafer;
4 means for testing a wafer metrology;
5 wherein said means for grinding, cleaning and testing are contained
6 within a single clean room environment; and
7 means for transferring said wafer between said means for grinding and
8 said means for cleaning, within said clean room environment.